

		Course title: <i>Simulation of the electronic circuits</i>		
Course code	Course status	Semester	Number of ECTS credits	Lecture hours
PA1105	Mandatory	I	5	2+0+2

Study program: Graduate academic studies, ELECTRICAL ENGINEERING, study program: Electronics, Telecommunications and Computer engineering (studies last for 4 semesters, 120 ECTS credits).	
Prerequisites: No prerequisites required.	
Course aims: Introduction to the automatic design of the electronic circuits at the level of projecting, simulation, verification and configuration of real PCB based or So C based systems.	
Teacher(s) first and last names: Ph.D. Radovan Stojanović – teacher	
Teaching method: Lectures (which include exercises), laboratory exercises, laboratory, consultation, individual project, main project, team work.	
Course synopsis:	
Preliminary weeks	Preparation and semester enrolment.
I week	Introduction: course description, methodology of the course, why ADEK?, Actual methodology for projecting.
II week	VHDL: basics, philosophy and history, design of the abstraction, principle, Exercise #1, Lab #1, Homework #1
III week	Hierarchical principle : Declaration, Modulus, libraries, integration, delays, Exercise #2, Lab #2, Homework #2
IV week	Data types: objects, attributes, operators, modeling, subroutines, Exercise #3, Lab #3, Homework #3,
V week	FPGA: overview, design flow, configuration, manufacturer.
VI week	FPGA design example I, FPGA design example II, Exercise #4, Lab #4, Homework #4.
VII week	Free week
VIII week	Spice (PSPICE), introduction, why PSPICE, development, textual, integral approach, examples int, soft.
IX week	Modulus, analyzes, code organisation, code examples, Exercise #5, Lab #5, Homework #5.
X week	An example of the integrated software, Cadence PSPICE student edition 9.1.
XI week	An example of the integrated software, Electronics workbench.
XII week	An example of the integrated software, Protel, Orcad.
XIII week	Migration from the Max+II to Quartus platform
XIV week	Basics of the system at the PCB and SoC
XV week	Examples of the integrated SoC projects
XVI week	<i>Final exam</i>
Final week XVIII-XXI week	Administrative procedures. Additional lessons, correction of the final exam and administrative procedures
STUDENT WORKLOAD	
<u>per week</u> 5 credits x 40/30 = 6 hours and 40 minutes Work hours structure: 2 hours for teaching 0 hour for exercises 2 hours for laboratory exercises 2 hours for individual work, team work including consultations.	<u>per semester</u> Teaching and the final exam: (6 h 40 min.) x 16 = 106 h 40 min. Necessary preparation (before semester): 2 x (6 h 40 min.) = 13 h 20 min. Total work hours for the course: 5 x 30 hours = 150 hours Additional hours for preparing correction of the final exam, including the exam taking - up to 30 hours (the rest of the time from the first two items, up to the total work hours for the course, 150 hours). Work hours structure: 106 h 40 min. (lectures) + 13 h 20 min. (preparation) + 30 hours (additional work)
Lessons attendance is mandatory for students, as well as doing home exercises, laboratory exercises and both tests.	
Literature: [1] R. Stojanovic, <i>Automatizovani Dizajn Elektronskih Kola (ADEK-CAED)</i> , Univerzitet Crne Gore, lecture notes, CD [2] Michael John Sebastian Smith, <i>Application-Specific Integrated Circuits</i> , Addison-Wesley, 1997 (ISBN: 0201500221)	
The forms of knowledge testing and grading: Lessons attendance and activities during the lessons (5 %) points, Laboratory (10 %). Test #1 i #2, 2x20% (40%). Practical project (20 %). Final exam (25%). Student gets the passing grade by collecting 50 points at least.	
Special remarks for the course:	
Teacher(s) who gave the information: PhD R. Stojanović	
Note: www.apeg.cg.yu (additional information about the course)	